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UTILITY PATENT APPLICATION TRANSMITTAL

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Attorney Docket No. 0819-408

First Inventor or Application Identifier: Hiroaki NAKAOKA et al.

Title: METHOD OF FABRICATING SEMICONDUCTOR DEVICE

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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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2. [X] Specification *Total Pages* [26]
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   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
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   - Claim(s)
   - Abstract of the Disclosure
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METHOD OF FABRICATING SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a MIS transistor having a polysilicon gate electrode provided on a gate insulating film and, more particularly, to an improvement in the driving force thereof.

Doping of the gate electrode of a MOS transistor with an impurity has been performed conventionally and commonly to reduce the resistance of the gate electrode and thereby improve the driving force of the MOS transistor. In particular, a CMOS device typically has a so-called dual gate structure in which the gate electrode of an n-channel MOS transistor is doped with an n-type impurity (phosphorus or arsenic) and the gate electrode of a p-channel MOS transistor is doped with a p-type impurity (boron).

However, since boron as the p-type impurity is particularly likely to be diffused in an oxide film, a phenomenon of so-called "boron penetration" is observed in which boron passes through the gate oxide film to enter the channel region of a Si substrate, which depletes the gate electrode. This causes the disadvantages of a lower driving force of the p-channel MOS transistor, degraded subthreshold characteristics, and aggravated short-channel effects.

To prevent these disadvantages, there has been used a technique for suppressing downward diffusion of boron by

composing the gate insulating film of a silicon oxynitride film. In using the technique, there has commonly adopted a method of forming a silicon oxynitride film directly on a silicon substrate by performing a heat treatment, while allowing a gas mixture of oxygen and NO or an N_2O gas to flow over the silicon substrate, or a method of changing a silicon oxide film already formed into a silicon oxynitride film by allowing an N_2O gas or NH_3 gas to flow over the silicon oxide film and thereby introducing nitrogen into the silicon oxide film.

However, as the gate length of a transistor becomes shorter with the increasing miniaturization and higher integration of a CMOS device currently pursued, a gate insulating film is also reduced in thickness to provide a sufficient driving force despite a reduction in voltage, which has caused the problem that a transistor with a sufficient driving force is not provided even if the gate insulating film is composed of a silicon oxynitride film.

Although the cause thereof has not been determined yet with certainty, the present inventors have experimentally assumed that an insufficient driving force is attributable to a mechanism other than the depletion of a gate electrode and, in particular, to a poor state of nitrogen distribution in the silicon oxynitride film as the gate insulating film.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method of fabricating a semiconductor device with a large driving force, such as a MIS transistor, while suppressing downward penetration of an impurity from a gate insulating film of the MIS transistor having a gate electrode doped with the impurity.

A method of fabricating a semiconductor device according to the present invention comprises the steps of: (a) forming a silicon oxynitride film on a substrate; (b) performing a heat treatment, while keeping a surface of the silicon oxynitride film in contact with a gas containing nitrogen, to introduce at least nitrogen into the silicon oxynitride film; and (c) forming a semiconductor film containing an impurity on the silicon oxynitride film.

In accordance with the method, nitrogen can be introduced additionally such that a nitrogen distribution having a steeply sloped configuration is produced in the silicon oxynitride film. This suppresses the entrance of nitrogen into the semiconductor film and the substrate, while suppressing the penetration of the impurity from the semiconductor film into the substrate. This allows a device formed by using the semiconductor film and the silicon oxynitride film to retain excellent characteristics. In a MIS transistor, e.g., a reduction in driving force assumedly caused by the penetration of nitrogen into the gate electrode or

the semiconductor substrate can be suppressed, while the penetration of the impurity from the gate electrode composed of the semiconductor film into the semiconductor substrate is suppressed. In summary, the suppression of the short-channel effects resulting from the penetration of the impurity is achievable simultaneously with an improvement in the driving force of the transistor.

In the method of fabricating a semiconductor device, the silicon oxynitride film is preferably formed by using an N_2O gas in the step (a).

In the method of fabricating a semiconductor device, the step (c) preferably includes the substeps of: forming, as the semiconductor film, an amorphous silicon film on the silicon oxynitride film; implanting impurity ions into the amorphous silicon film; and performing a heat treatment for activating the impurity to change the amorphous film into a polysilicon film. This suppresses the penetration of the impurity into the substrate underlying the silicon oxynitride film by using a high impurity holding capability of the amorphous silicon film.

In the method of fabricating a semiconductor device, the heat treatment is preferably performed at 800 to 1050 ℃ in the step (b).

In the method of fabricating a semiconductor device, a gas containing nitrogen and oxygen is preferably used as the gas containing nitrogen in the step (b).

In that case, it was found that a particularly large effect was achievable by using an NO gas as the gas containing nitrogen.

Alternatively, an N_2O gas can also be used as the gas containing nitrogen.

In the method of fabricating a semiconductor device, if the semiconductor device is a p-channel MIS transistor, a MIS transistor having a high driving force suitable for a CMIS device with a dual gate structure is obtainable by forming a gate electrode containing boron in the step (c).

BRIEF DESCRIPTION OF THE DRAWINGS

Figures **1(a)** to **(e)** are cross-sectional views illustrating the first half steps of the process of fabricating a semiconductor device according to an embodiment of the present invention;

Figures **2(a)** to **(c)** are cross-sectional views illustrating the second half steps of the process of fabricating a semiconductor device according to the embodiment of the present invention;

Figures **3** show respective short-channel characteristics in a conventional p-channel MIS transistor and in a p-channel MIS transistor according to the present embodiment;

Figures **4** show respective Ion-Ioff characteristics in the conventional p-channel MIS transistor and in the p-channel MIS transistor according to the present embodiment;

Figure **5** shows respective subthreshold characteristics in

the conventional p-channel MIS transistor and in the p-channel MIS transistor according to the present embodiment;

Figure **6** shows respective transconductance characteristics in the conventional p-channel MIS transistor and in the p-channel MIS transistor according to the present embodiment;

Figure **7** shows, on a logarithmic scale, the results of measuring, by SIMS, the distributions of nitrogen concentration in silicon oxynitride films and their vicinities according to Example and Comparative Examples; and

Figure **8** shows, on a linear scale, the results of measuring, by SIMS, the distributions of nitrogen concentration in the silicon oxynitride films and their vicinities according to Example and Comparative Examples.

DETAILED DESCRIPTION OF THE INVENTION

Figures **1(a)** to **(e)** and Figures **2(a)** to **(c)** are cross-sectional views illustrating the process of fabricating a semiconductor device (CMOS device) according to an embodiment of the present invention. Throughout the drawings, Rp denotes a region in which a p-channel MIS transistor is to be formed and Rn denotes a region in which an n-channel MIS transistor is to be formed.

In the step shown in Figure **1(a)**, trench isolation regions **11** surrounding the p-channel MIS transistor formation region Rp and the n-channel MIS transistor formation region Rn are formed

in a Si substrate **10**. Then, the Si substrate **10** is kept in contact with an N_2O gas at a temperature of about 1000 ℃ for about 60 sec, whereby a silicon oxynitride film **12** with a thickness of 2.8 nm is formed on the substrate **10**.

It is to be noted that the method of forming the silicon oxynitride film is not limited thereto. For example, it is also possible to perform a heat treatment at about 1000 ℃, while keeping the surface of the Si substrate **10** in contact with a gas mixture of an NO gas and an O_2 gas. Alternatively, it is also possible to form a silicon oxide film and introduce nitrogen into a surface of the silicon oxide film.

Next, in the step shown in Figure **1(b)**, nitrogen (N) is introduced into the interior of the silicon oxynitride film **12** by performing a heat treatment at 900 ℃ for 30 sec, while keeping the silicon oxynitride film **12** in contact with an NO gas. As a consequence, the state of nitrogen distribution in the silicon oxynitride film **12** changes such that not only nitrogen concentration in the silicon oxynitride film **12** increases but also a peak portion at which nitrogen concentration is maximum exists at a center portion in the direction of thickness of the silicon oxynitride film **12** and the distribution of nitrogen exhibits a steeply sloped configuration.

Next, in the step shown in Figure **1(c)**, a semiconductor film **13** for gate electrode composed of an amorphous silicon film is deposited on the silicon oxynitride film **12**.

Next, in the step shown in Figure **1(d)**, a photoresist film **21** covering the n-channel MIS transistor formation region Rn is formed on the semiconductor film **13** for gate electrode. By using the photoresist film **21** as a mask, boron ions (B^+) are implanted into the semiconductor film **13** for gate electrode at an implant energy of 5 keV and a dose of $5 \times 10^{15}/cm^2$, thereby changing, into the p type, the portion of the semiconductor film **13** for gate electrode located in the p-channel MIS transistor formation region Rp.

Next, in the step shown in Figure **1(e)**, the photoresist film **21** is removed. Then, a photoresist film **22** covering the p-channel MIS transistor formation region Rp is formed on the semiconductor film **13** for gate electrode. By using the photoresist film **22** as a mask, phosphorus ions (P^+) are implanted into the semiconductor film **13** for gate electrode at an implant energy of 10 keV and a dose of $7 \times 10^{15}/cm^2$, thereby changing, into the n type, the portion of the semiconductor film **13** for gate electrode located in the n-channel MIS transistor formation region Rn.

Next, in the step shown in Figure **2(a)**, a silicon nitride film with a thickness of about 150 nm is deposited on the semiconductor film **13** for gate electrode. The silicon nitride film and the polysilicon film are patterned by photolithography and dry etching, thereby forming gate electrodes **13a** and **13b** and on-gate protective layers **14a** and **14b** in the p-channel MIS transistor formation region Rp and in the n-channel MIS transistor

formation region Rn, respectively. By using the gate electrodes **13a** and **13b** and the on-gate protective layers **14a** and **14b** as a mask, boron as a low-concentration p-type impurity is ion implanted into the p-channel MIS transistor formation region Rp, while arsenic as a low-concentration n-type impurity is ion implanted into the n-channel MIS transistor formation region Rn, whereby low-concentration source/drain regions (or extension regions) **20a** and **20b** are formed in the Si substrate **10**.

Next, in the step shown in Figure **2(b)**, a silicon oxide film **15** with a thickness of about 15 nm and a silicon nitride film **16** with a thickness of about 55 nm are deposited successively.

Next, in the step shown in Figure **2(c)**, anisotropic etching is performed with respect to the silicon nitride film **16** and the silicon oxide film **15**, thereby forming oxide film sidewalls **15a** and **15b** each having an L-shaped cross section on respective side surfaces of the gate electrodes **13a** and **13b** and of the on-gate protective layers **14a** and **14b** and forming nitride film sidewalls **16a** and **16b** covering the side and bottom surfaces of the oxide film sidewalls **15a** and **15b**. During the anisotropic etching, the silicon oxynitride film **12** is also patterned to form gate insulating films **12a** and **12b** made of a silicon oxynitride under the gate electrodes **13a** and **13b** and the like.

Thereafter, by using the gate electrodes **13a** and **13b**, the on-gate protective layers **14a** and **14b**, the oxide film sidewalls **15a** and **15b**, and the nitride film sidewalls **16a** and **16b** as a mask,

high-concentration boron is ion implanted into the portion of the Si substrate **10** located in the p-channel MIS transistor formation region Rp and high-concentration arsenic is ion implanted into the portion of the Si substrate **10** located in the n-channel MIS transistor formation region Rn, whereby high-concentration source/drain regions **21a** and **21b** are formed. Subsequently, a heat treatment (RTA) is performed at 1000 ℃ for 10 sec to activate the impurities in the low-concentration source/drain regions **20a** and **20b** and in the high-concentration source/drain regions **21a** and **21b**.

By the foregoing process, there is formed a CMOS device with a so-called dual gate structure in which the conductivity types of the respective impurities contained in the gate electrodes **13a** and **13b** are coincident with those of the respective channels of the transistors.

Although the depiction of the subsequent fabrication process is omitted, an interlayer insulating film is deposited over the substrate and planarized, contact holes reaching the high-concentration source/drain regions are formed in the interlayer insulating film, and a metal such as W or Al is buried in the contact holes to form metal plugs. A wiring layer is further formed thereon and, if necessary, a multilayer wiring structure is formed by repeating the formation of the interlayer insulating film, the metal plugs, and the wiring layer.

When the heat treatment at a temperature exceeding about

600 ℃ is performed after the steps shown in Figures **1(d)** and **(e)**, each of the gate electrodes **13a** and **13b** (semiconductor film **13** for gate electrode) changes from the amorphous silicon film to the polysilicon film. If the heat treatment for impurity activation is performed immediately after the completion of the step shown in Figure **1(e)**, a change from the amorphous silicon film to the polysilicon film occurs. Even if the heat treatment for impurity activation is not performed, there are cases where the change from the amorphous silicon film to the polysilicon film is caused by a CVD process for depositing the silicon oxide film **15** and the silicon nitride film **16** shown in Figure **2(b)** or by the heat treatment for impurity activation in the step shown in Figure **2(c)**.

The method of fabricating a semiconductor device according to the present invention is characterized in that annealing (heat treatment) is performed by keeping the silicon oxynitride film **12** in contact with the NO gas in the step shown in Figure **1(b)**. It has been found that the treatment increases the nitrogen concentration in the silicon oxynitride film **12** and provides the nitrogen distribution in a steeply sloped configuration. The profile of the nitrogen concentration will be described later. As a result of conducting evaluation, the present inventors have found that such an NO gas annealing process provides the following characteristics which are different from the characteristics of the conventional p-channel MIS transistor.

Figure **3(a)** shows the short-channel characteristics of a conventional p-channel MIS transistor and Figure **3(b)** shows the short-channel characteristics of the p-channel MIS transistor according to the present embodiment. The conventional p-channel MIS transistor has the structure shown in Figure **2(c)** in which a silicon oxynitride film that has not been subjected to gas annealing is used as a gate insulating film. In each of Figures **3(a)** and **(b)**, the horizontal axis represents a gate length (μm) and the vertical axis represents a threshold voltage (V). The numerals shown in the upper left portions of the Figures **3(a)** and **(b)** indicate the dose of ions implanted in the channel region (i.e., the dose of ions implanted for threshold control). For example, "4e12" indicates that the dose of the implanted ions is "$4 \times 10^{12}/cm^2$".

From the comparison between Figures **3(a)** and **(b)**, it will be understood that the threshold voltage of the p-channel MIS transistor according to the present embodiment is barely reduced compared with that of the conventional p-channel MIS transistor provided that the gate lengths thereof are the same. This may be because the threshold voltage of the conventional p-channel MIS transistor is reduced by the penetration of boron from the gate electrode into the substrate. By contrast, boron penetration is suppressed effectively in the p-channel MIS transistor according to the present embodiment.

Figure **4(a)** shows the Ion-Ioff characteristics of the

conventional p-channel MIS transistor and Figure **4(b)** shows the Ion-Ioff characteristics of the p-channel MIS transistor according to the present embodiment. The conventional p-channel MIS transistor has the structure shown in Figure **2(c)** in which the silicon oxynitride film that has not been subjected to gas annealing is used as the gate insulating film. In each of Figures **4(a)** and **(b)**, the horizontal axis represents an on-state current Ion (μA/μm) and the vertical axis represents an off-state leakage current Ioff (A/μm). Each of Ion and Ioff indicates a source-to-drain current. The numerals, such as "4e12", shown in the upper left portions indicate the same as described above.

As shown in Figure **4(a)**, if the threshold voltage of the p-channel MIS transistor with the conventional structure is adjusted such that the off-state leakage current Ioff is 1 nA/μm (per unit gate width) when the concentration of the impurity for threshold control is varied, the on-state current Ion is about 100 (μA/μm) (see the arrow in Figure **4(a)**). On the other hand, if the threshold voltage of the p-channel MIS transistor according to the present embodiment is adjusted such that the off-state leakage current Ioff is 1 nA/μm (per unit gate width) when the concentration of the impurity for threshold control is varied, the on-state current Ion is about 250 (μA/μm) (see the arrow in Figure **4(b)**). In summary, the p-channel MIS transistor according to the present embodiment has higher on-off characteristics and a larger driving force.

Figure **5** shows the respective subthreshold characteristics (Vg-Id characteristics) of the conventional p-channel MIS transistor and the p-channel MIS transistor according to the present embodiment. The conventional p-channel MIS transistor has the structure shown in Figure **2(c)** in which the silicon oxynitride film that has not been subjected to gas annealing is used as the gate insulating film. In Figure **5**, the horizontal axis represents a gate voltage Vg (V) and the vertical axis represents a drain current Id (A).

As can be seen from Figure **5**, the p-channel MIS transistor according to the present embodiment has a smaller off-state leakage current and a Vg-Id characteristic curve with sharper inclination. From the results of the experiments, it will be understood that the p-channel MIS transistor according to the present embodiment has superior on-off characteristics.

Figure **6** shows the respective transconductance characteristics (Gm-Vg characteristics) of the conventional p-channel MIS transistor and the p-channel MIS transistor of the present embodiment. The conventional p-channel MIS transistor has the structure shown in Figure **2(c)** in which the silicon oxynitride film that has not been subjected to gas annealing is used as the gate insulating film. In Figure **6**, the horizontal axis represents a gate voltage Vg (V) and the vertical axis represents a transconductance Gm (S).

As can be seen from Figure **6**, the p-channel MIS transistor

according to the present embodiment has transconductance with a larger maximum value, i.e., superior switching properties.

A consideration will be given to the reason that the driving force of the p-channel MIS transistor is improved by the fabrication method according to the present embodiment.

A conventional silicon oxynitride film is formed by the same treatment as performed in the step shown in Figure **1(a)**. That is, the conventional silicon oxynitride film is formed by, e.g., performing a heat treatment at a temperature of about 1000 ℃, while keeping a Si substrate in contact with a gas mixture of NO and O_2 (or an N_2O gas) or by performing a heat treatment (RTA) at a temperature of about 1000 ℃, while keeping a silicon oxide film in contact with N_2 or NH_3. However, it has been found that, if the silicon oxynitride film formed by such a treatment is used as a gate insulating film that has been reduced particularly in thickness in recent years, the driving force of a p-channel MIS transistor is reduced disadvantageously.

Although the cause thereof has not been determined yet with certainty, it is assumed to be the scattering of carriers caused by an interface state density due to excess nitrogen atoms present at an interface immediately overlying a channel region, an increase in dangling voids resulting from the breakage of bonds in a silicon oxide film by nitrogen atoms, or an increase in gate resistance due to excess nitrogen atoms present in a gate electrode.

If the amount of nitrogen introduced into the silicon oxide film is reduced, the penetration of boron from the gate electrode into the channel region cannot be prevented reliably, so that the gate electrode is depleted to reduce the driving force or aggravate short-channel effects including a reduction in threshold voltage. Thus, it is difficult to simultaneously achieve an improvement in the driving force of the transistor and the suppression of the short-channel effects so that, under present circumstances, a trade-off therebetween is determined individually for a CMOS device depending on the type thereof.

However, the present inventors found experimentally that, if the heat treatment was performed while the surface of the silicon oxynitride film was exposed to the NO gas (NO gas annealing), the suppression of the short-channel effects was achievable simultaneously with improvements in the driving force of the transistor (including an improvement in on-off characteristics and an improvement in transconductance). The present inventors further examined changes that had been caused by the NO gas annealing in distributions of nitrogen concentration in the individual portions of the transistor.

Figures **7** and **8** shows the results of measuring, by SIMS, the distributions of nitrogen concentration (atoms/cm^3) in the silicon oxynitride films and their vicinities according to Example and Comparative Examples. In Figure **7**, the horizontal axis represents the direction of depth in cross section and the

vertical axis represents nitrogen concentration (on a logarithmic scale). Figure **8** shows the same data as shown in Figure **7** by using a linear scale to express the concentration which is represented by the vertical axis. In each of the drawings, ①, ②, ③, ⑤, and ⑦ indicate samples prepared by the following treatments in each of which amorphous silicon is deposited on a silicon oxynitride film with a thickness of 2.6 nm.

① : Comparative Example 1

The sample was prepared by performing a heat treatment at 1000 ℃, while keeping a surface of a Si substrate as an underlie in contact with an N_2O gas, and thereby oxynitriding silicon to form an oxynitride film (the conventional p-channel MOS transistor in a mid-step of the fabrication process from which the data shown in Figures **4(a)** and Figures **5** and **6** was obtained).

②: Comparative Example 2

The sample was prepared by performing a heat treatment at 1000 ℃, while keeping a surface of a Si substrate as an underlie in contact with an N_2O gas, thereby oxynitriding silicon to form an oxynitride film (prepared by further performing a heat treatment at 800 ℃, while keeping a surface of the sample of Comparative Example 1 in contact with an NO gas (NO gas annealing)).

③: Example

The sample was prepared by performing a heat treatment at 1000 ℃, while keeping a surface of a Si substrate as an underlie in contact with an N_2O gas, thereby oxynitriding silicon to form an oxynitride film (prepared by further performing a heat treatment at 900 ℃, while keeping a surface of the sample of Comparative Example 1 in contact with an NO gas (NO gas annealing)).

⑤ : Comparative Example 3

The sample was prepared by performing a heat treatment, while keeping a surface of a Si substrate as an underlie in contact with a gas mixture of O_2 and NO (containing 30% of NO gas), and thereby oxynitriding silicon to form an oxynitride film.

⑦ : Comparative Example 4

The sample was prepared by performing a heat treatment, while keeping a surface of a Si substrate as an underlie in contact with a gas mixture of O_2 and NO (containing 10% of NO), and thereby oxynitriding silicon to form an oxynitride film.

In each of Figures **7** and **8**, "a-Si" indicates an amorphous silicon film, "SiON" indicates a silicon oxynitride film, and "Si-sub" indicates a Si substrate. The two broken lines in each of the drawings represents the interface between the amorphous

silicon film and the silicon oxynitride film and the interface between the silicon oxynitride film and the Si substrate.

As shown in Figure **8**, the nitrogen concentration in the sample ①, which was the conventional silicon oxynitride film prepared in Comparative Example 1, has a peak at a point close to the interface between the silicon oxynitride film and the Si substrate. Since the distribution of nitrogen concentration presents a gently sloped configuration, if the impurity concentration is increased to such a degree as to prevent the penetration of the impurity, the nitrogen concentration in the amorphous silicon film and in the Si substrate is expected to be higher.

By contrast, the nitrogen concentration in the sample ③ prepared in Example in accordance with the method of the present embodiment has a peak value at a point located adjacent the middle portion of the silicon oxynitride film and the distribution of nitrogen concentration presents a steeply sloped configuration. The nitrogen concentration in the silicon oxynitride film of the sample ③ of Example is about 8 atom%. It has also been proved that, if the peak of the nitrogen concentration in the silicon oxynitride film has a value on the order of the peak value in the sample ③ of Example shown in Figure **8**, the penetration of boron can be prevented. If the nitrogen concentration is excessively higher than 8 atom%, the transistor characteristics may be adversely affected.

If NO gas annealing is performed at 800 ℃ as in the sample ② of Comparative Example 2, the peak of the nitrogen concentration remains at a point adjacent the interface between the silicon oxynitride film and the Si substrate, so that the configuration of the distribution is not steeply sloped, either. As a result of forming a MIS transistor from the sample of Comparative Example 2, it was found that the driving force was lower than that of a MIS transistor formed from the sample ③ of Example.

When the temperature for performing NO gas annealing with respect to a silicon oxynitride film was set to 1000 ℃, though the data obtained at that temperature is not shown in Figures **7** and **8**, it was found that the configuration of the distribution is more steeply sloped than in the sample ① of Example and characteristics associated with the short-channel effects, driving force, and the like of the MIS transistor were excellent.

In the case of forming a silicon oxynitride film directly from a Si substrate by using a gas mixture of O_2 and NO containing NO in a high proportion, as in the sample ⑤ of Comparative Example 3, the peak of the nitrogen concentration is located at a nearly middle portion in the direction of thickness of the silicon oxynitride film but the nitrogen concentration is higher in a portion closer to the amorphous silicon film. As a result of forming a MIS transistor from the sample ⑤ of Comparative Example 3, it was found that the driving force was lower than that of a

MIS transistor formed from the sample ③ of Example.

From the foregoing results, it can be considered that, by performing the NO gas annealing of the present invention with respect to a silicon oxynitride film, the nitrogen concentration is distributed into a steeply sloped configuration such that nitrogen exists at a high concentration in the silicon oxynitride film, which suppresses the penetration of boron into the Si substrate **10** and provides a high driving force.

In the conventional step of forming a silicon oxynitride film, the silicon oxynitride film is formed directly from the silicon substrate or by nitriding the silicon oxide film. In accordance with the conventional method, however, the distribution of nitrogen concentration in the silicon oxynitride film has a gently sloped configuration. Since nitrogen is distributed continuously not only in the silicon oxynitride film but also in the gate electrodes (amorphous silicon film) on both sides and in the Si substrate, the gently sloped distribution of nitrogen concentration leads to the entrance of nitrogen at a relatively high concentration into the gate electrodes and also into the Si substrate if nitrogen at a concentration required to suppress boron penetration is to be contained in the silicon oxynitride film. As a result, the driving force of the transistor is assumedly reduced by an increase in gate resistance in the gate electrodes or by a reduction in the mobility of carriers in the channel region of the Si substrate.

If the nitrogen concentration has a peak at a point adjacent the interface with the Si substrate, in particular, the probability is high that the driving force of the transistor has been reduced by an increased nitrogen concentration in the Si substrate.

By contrast, the present embodiment allows additional introduction of high-concentration nitrogen by performing NO gas annealing with respect to the silicon oxynitride film, while providing a steeply sloped nitrogen distribution in the silicon oxynitride film. As a consequence, the driving force of the transistor can be held high, while the short-channel effects are suppressed by effectively preventing boron penetration. In summary, the suppression of the short-channel effects in a p-channel MIS transistor is achievable simultaneously with an improvement in driving force.

Judging from the results of the experiments conducted by the present inventors, the heat treatment temperature during the NO gas annealing is preferably higher than 800 ℃ and not higher than 1050 ℃.

The structure of the p-channel MIS transistor is not limited to a SAC structure as shown in Figure **2(c)**. However, since the stress resulting from the nitride film sidewalls **16a** is exerted on the gate electrodes **13a** or the like in the p-channel MIS transistor with the SAC structure shown in Figure **2(c)**, boron in the gate electrodes **13a** is particularly likely to enter the Si

substrate **10**. By applying the present invention to the p-channel MIS transistor with the SAC structure, therefore, a structure particularly suitable for miniaturization is obtained.

OTHER EMBODIMENTS

Although the foregoing embodiment has performed annealing while keeping the surface of the silicon nitride film in contact with the NO gas (NO gas annealing), effects equal to those achieved in the foregoing embodiment are also achievable by performing annealing while keeping a silicon oxynitride film in contact with another gas containing oxygen and nitrogen, such as an N_2O gas or NO_2 gas.

Although the foregoing embodiment has described the annealing process in the case of using the silicon oxynitride film as a gate insulating film provided under the gate electrode of the MIS transistor, the present invention is not limited to such an embodiment and is also applicable to a device such as a MIS capacitor or a TFT transistor.

The present invention is also applicable to a MIS transistor or MIS capacitor using a SOI substrate.

WHAT IS CLAIMES IS:

1. A method of fabricating a semiconductor device, the method comprising the steps of:

(a) forming a silicon oxynitride film on a substrate;

(b) performing a heat treatment, while keeping a surface of the silicon oxynitride film in contact with a gas containing nitrogen, to introduce at least nitrogen into the silicon oxynitride film; and

(c) forming a semiconductor film containing an impurity on the silicon oxynitride film.

2. The method of claim 1, wherein the silicon oxynitride film is formed by using an N_2O gas in the step (a).

3. The method of claim 1, wherein the step (c) includes the substeps of:

forming, as the semiconductor film, an amorphous silicon film on the silicon oxynitride film;

implanting impurity ions into the amorphous silicon film; and

performing a heat treatment for activating the impurity to change the amorphous film into a polysilicon film.

4. The method of claim 1, wherein the heat treatment is performed at 800 to 1050 ℃ in the step (b).

5. The method of claim 1, wherein a gas containing nitrogen and oxygen is used as the gas containing nitrogen in the step (b).

6. The method of claim 5, wherein an NO gas is used as the

gas containing nitrogen in the step (b).

7. The method of claim 5, wherein an N_2O gas is used as the gas containing nitrogen in the step (b).

8. The method of any one of claims 1 to 7, wherein the semiconductor device is a p-channel MIS transistor and a silicon film for a gate electrode containing boron is formed in the step (c).

ABSTRACT OF THE DISCLOSURE

A silicon oxynitride film is formed on a substrate. Then, a heat treatment is performed, while keeping a surface of the silicon oxynitride film in contact with a gas containing nitrogen, such as an NO gas, to introduce at least nitrogen into the silicon oxynitride film and produce a steeply sloped distribution of nitrogen. A semiconductor film containing an impurity, such as an amorphous silicon film, is formed on the silicon oxynitride film. By forming a CMOS device with, in particular, a dual gate structure which comprises p-type and n-type MIS transistors each having a gate oxide film composed of the silicon oxynitride film and a gate electrode composed of a polysilicon film, a high driving force is provided, while boron penetration in the p-type MIS transistor is suppressed.

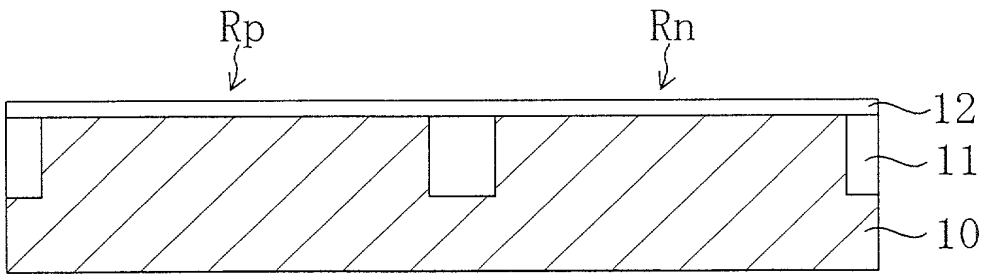


Fig. 1(a)

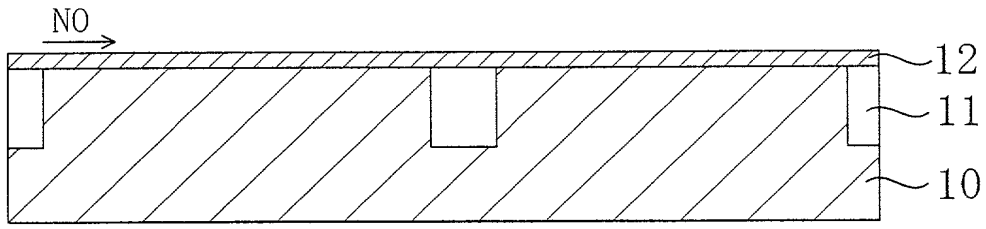


Fig. 1(b)

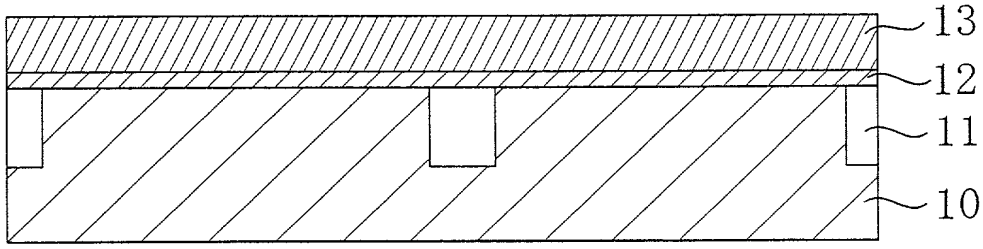


Fig. 1(c)

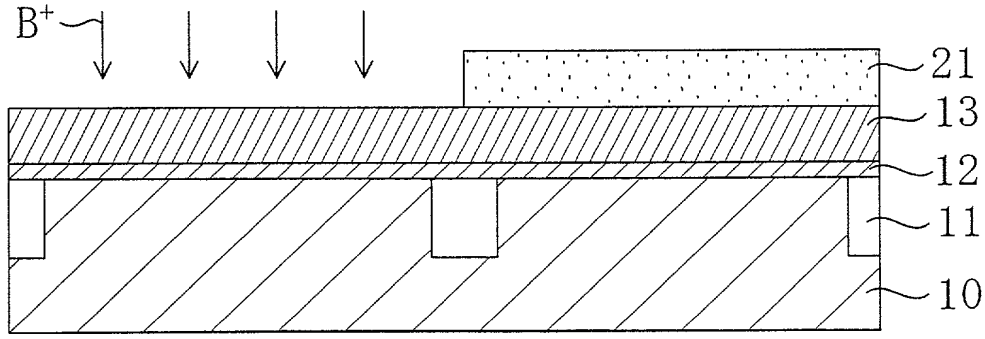


Fig. 1(d)

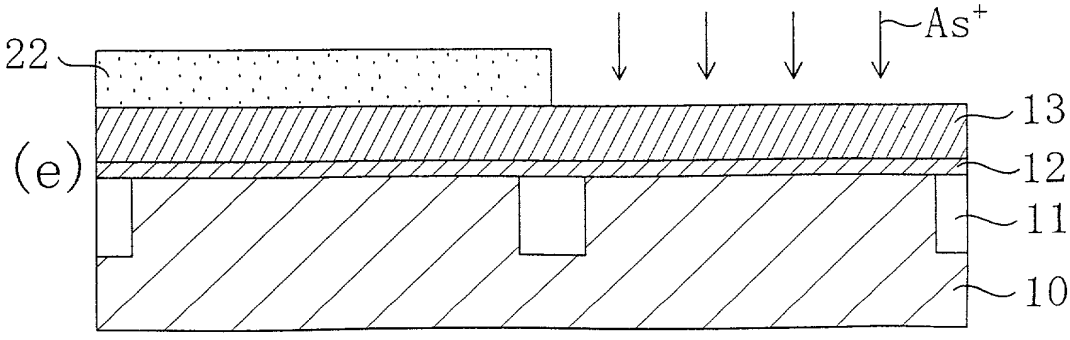


Fig. 1(e)

Fig. 2(a)

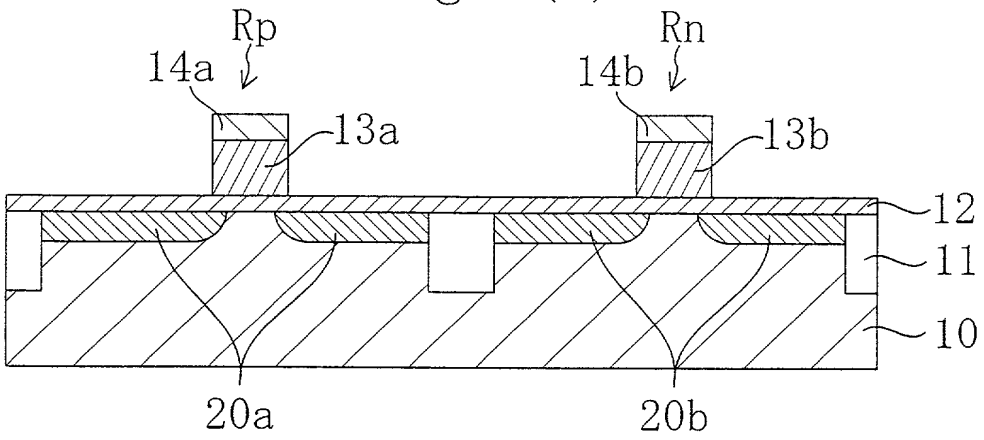


Fig. 2(b)

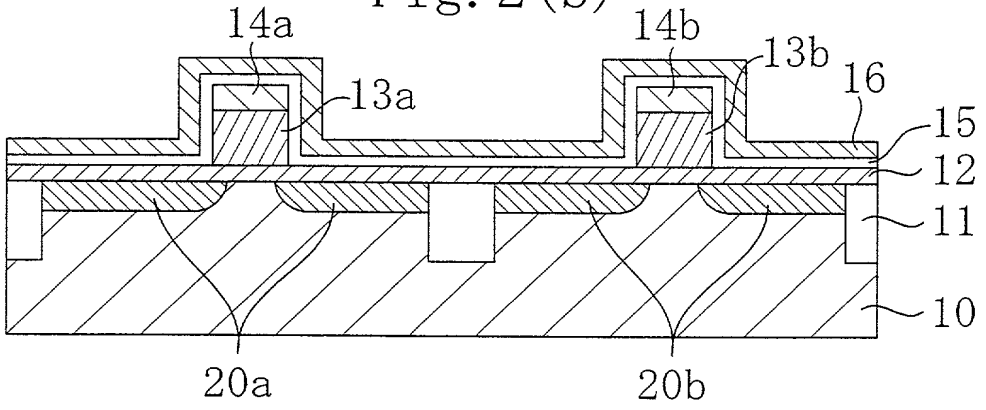


Fig. 2(c)

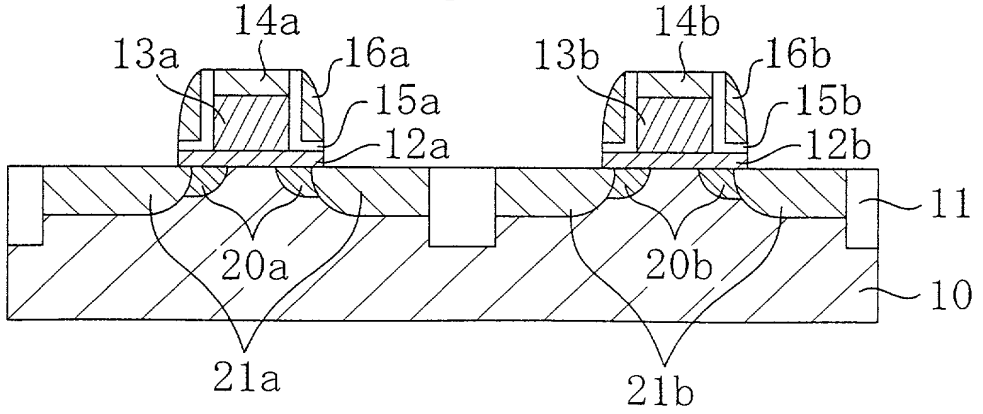


Fig. 3(a)

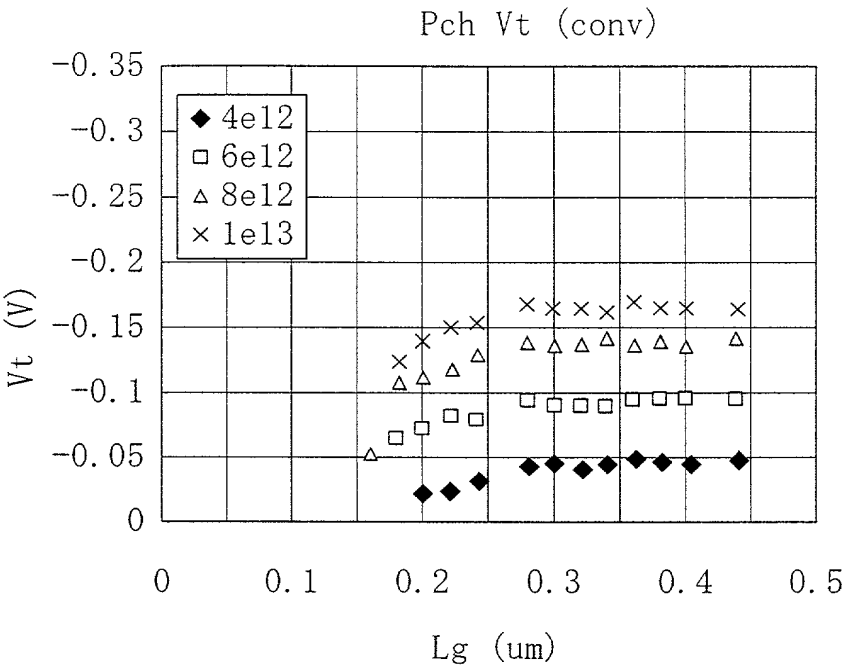

Pch Vt (conv)
-0.35
-0.3
-0.25
-0.2
-0.15
-0.1
-0.05
0
Vt (V)
4e12
6e12
8e12
1e13
0
0.1
0.2
0.3
0.4
0.5
Lg (um)

Fig. 3(b)

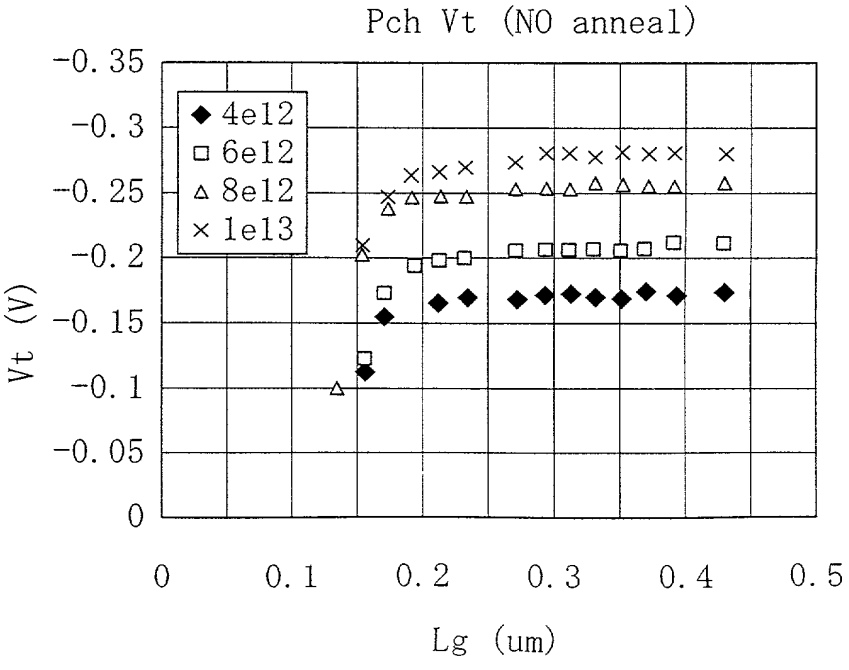

Pch Vt (NO anneal)
-0.35
-0.3
-0.25
-0.2
-0.15
-0.1
-0.05
0
Vt (V)
4e12
6e12
8e12
1e13
0
0.1
0.2
0.3
0.4
0.5
Lg (um)

Fig. 4(a)

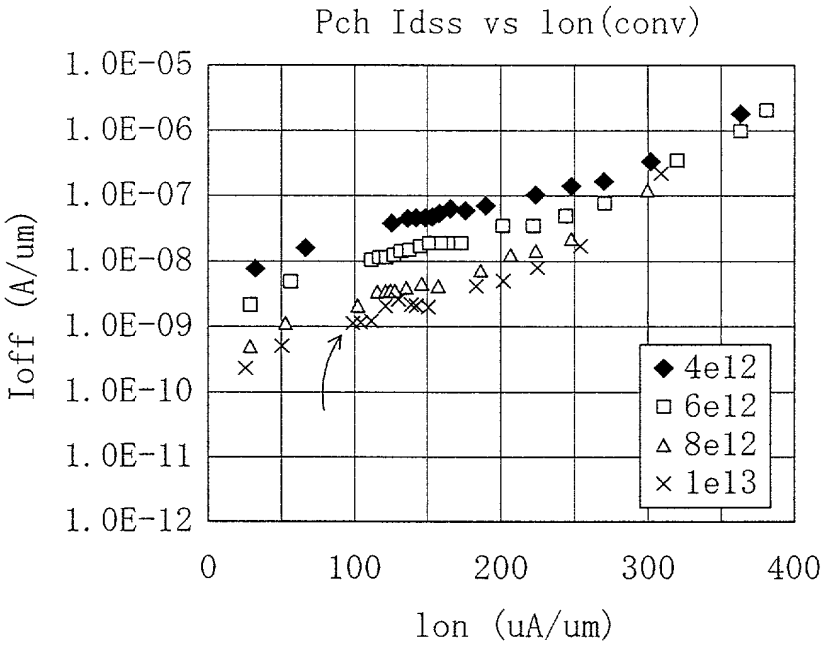

Pch Idss vs Ion(conv)
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
1.0E-11
1.0E-12
Ioff (A/um)
0
100
200
300
400
Ion (uA/um)
4e12
6e12
8e12
1e13

Fig. 4(b)

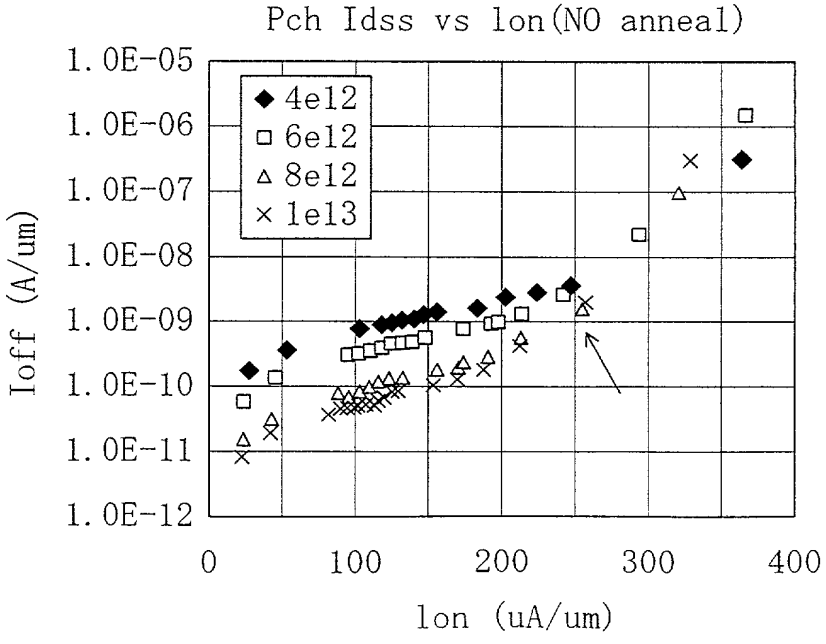
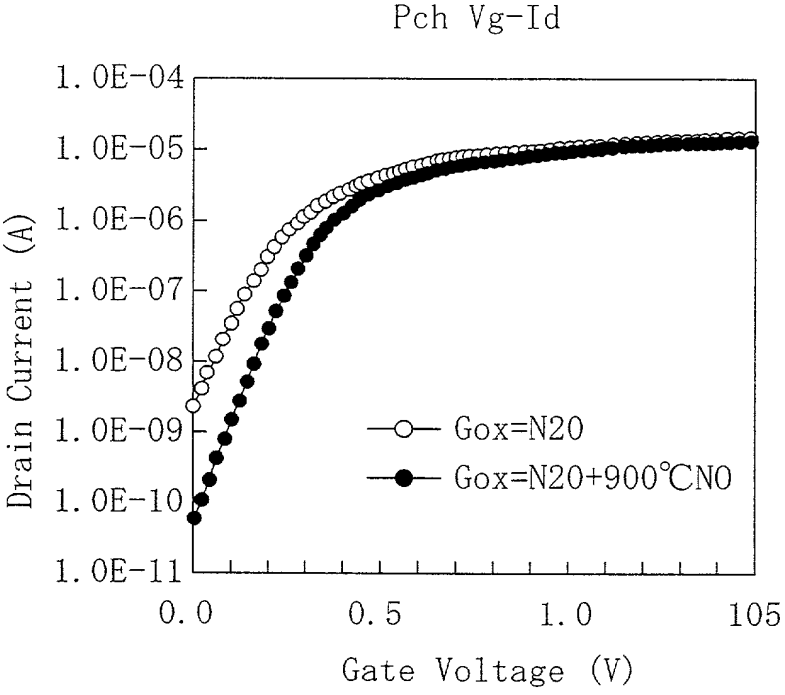

Pch Idss vs Ion(NO anneal)
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
1.0E-11
1.0E-12
Ioff (A/um)
0
100
200
300
400
Ion (uA/um)
4e12
6e12
8e12
1e13

Fig. 5


Pch Vg-Id
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1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
1.0E-11
Drain Current (A)
Gox=N20
Gox=N20+900℃NO
0.0
0.5
1.0
105
Gate Voltage (V)

Fig. 6

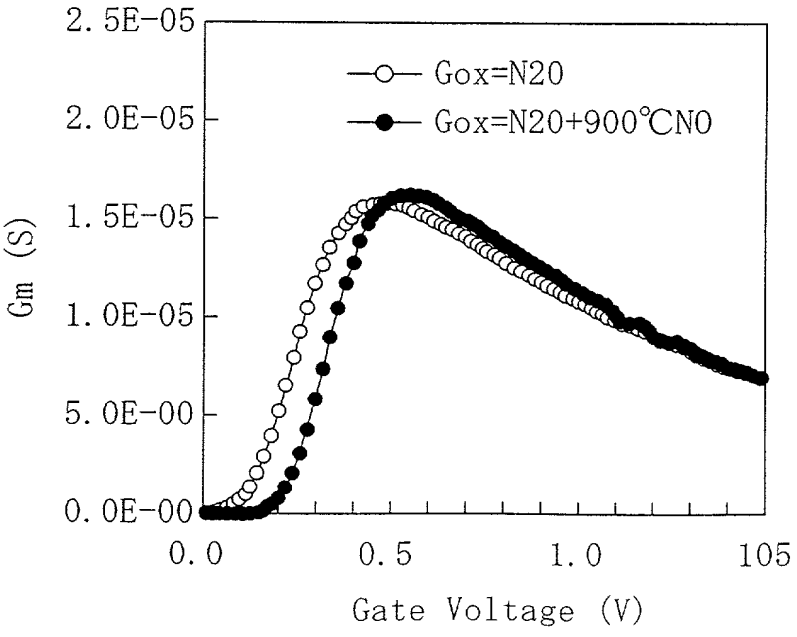

Pch Gm-Vg
2.5E-05
2.0E-05
1.5E-05
1.0E-05
5.0E-00
0.0E-00
Gm (S)
Gox=N20
Gox=N20+900℃NO
0.0
0.5
1.0
105
Gate Voltage (V)

Fig. 7

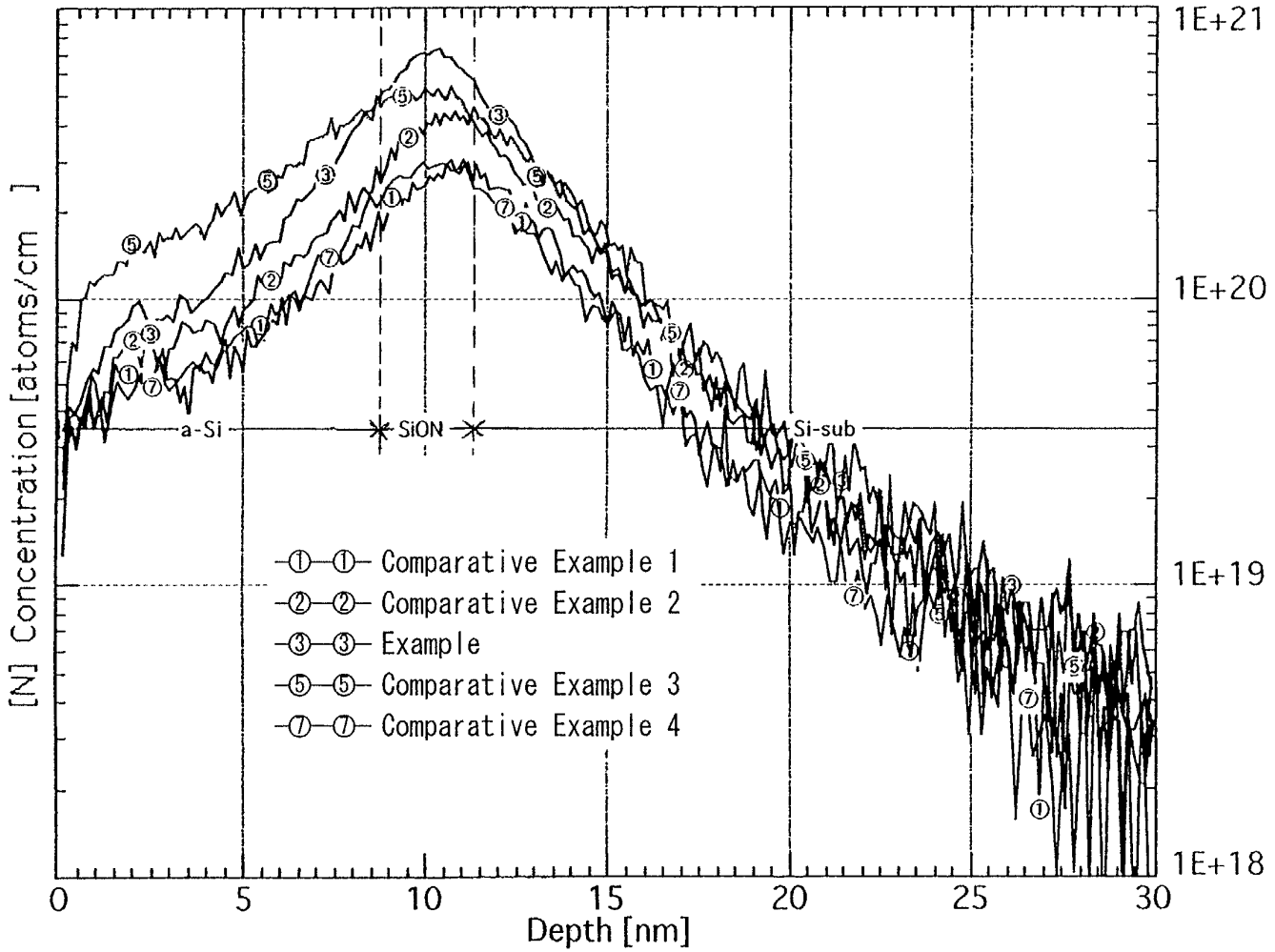
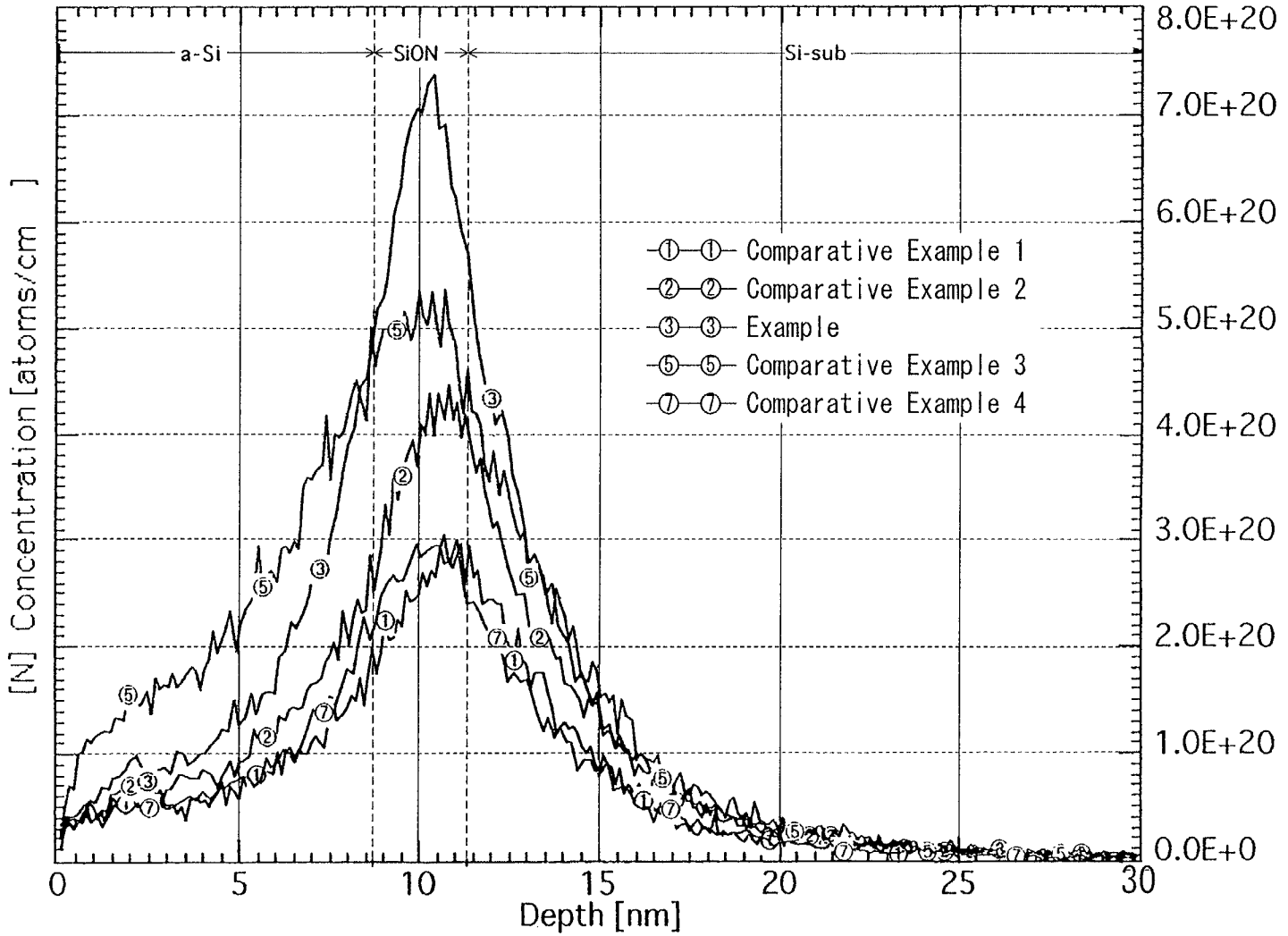

[N] Concentration [atoms/cm]
1E+21
1E+20
1E+19
1E+18
0
5
10
15
20
25
30
Depth [nm]
a-Si
SiON
Si-sub
①—①— Comparative Example 1
②—②— Comparative Example 2
③—③— Example
⑤—⑤— Comparative Example 3
⑦—⑦— Comparative Example 4

Fig. 8



DECLARATION AND POWER OF ATTORNEY FOR **PATENT** APPLICATION

Attorney Docket No.

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: **METHOD OF FABRICATING SEMICONDUCTOR DEVICE**, the specification of which is attached hereto unless the following box is checked:

[ ] The specification was filed on
and was assigned Serial No. (if known)

and was amended on (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s) (Number)	(Country)	(Month/Day/Year Filed)	Priority Claimed Yes	No
11-236792	Japan	08/24/1999	X	

All foreign applications, if any, for any Patent or Inventor's Certificate filed more than 12 months prior to the filing date of this application:

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, § 119(e) or § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status: patented, pending, abandoned

I hereby appoint the following attorneys to prosecute this application and/or any international application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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FULL NAME OF SIXTH JOINT INVENTOR (if any)	INVENTOR'S SIGNATURE	DATE
RESIDENCE (City, State & Country)		CITIZENSHIP
POST OFFICE ADDRESS (Complete Address including City, State & Country)		